HIGH SPEED HARDWARE IMPLEMENTATION OF A HEURISTIC 2D RECTANGLE PLACEMENT ALGORITHM

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Abstract

Many areas of industry involve computationally intensive layout design problems. A high performance computing system for swiftly generating and analyzing layout alternatives is much desired. The performance of such a system is largely affected by the efficiency of the placement algorithm and its degree of parallelism, and the employed hardware platform. In this paper, we present parallelization and high speed hardware implementation of a heuristic 2D rectangle placement algorithm. A performance analysis and evaluation of the suggested mapping onto reconfigurable hardware is also presented.

Keywords

Reconfigurable computing, Parallel Processing, Hardware Design, Layout Design, Placement Heuristics.