OPTIMIZING FIR FILTER MAPPING ON THE MORPHOSYS RECONFIGURABLE SYSTEM

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ABSTRACT

This paper proposes an optimized mapping of the FIR filter algorithm that enhances the rate of a reconfigurable computer over a basic mapping previously proposed [1]. It also presents a new interconnection scheme in the reconfigurable part of MorphoSys, a reconfigurable computing system [2]. Reconfigurable computing (RC) is introduced, followed by the MorphoSys RC system. Two optimized FIR mappings are then presented which deliver enhanced speed. A spreadsheet model will detail the modification and the improvement. The speedup achieved is also explained as well as the advantages in the mapping of the application.

Keywords: FIR Filter, Digital Signal Processing, MorphoSys, Reconfigurable Computing