NEW DIGITAL CODING ALGORITHMS UNDER MORPHOSYS

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ABSTRACT

At one extreme of the computing spectrum, we have general-purpose processors that are programmed entirely through software. At the other extreme are application-specific ICs (ASICS) that are custom designed for particular applications. General-purpose processors are designed to execute any application. On the other hand, ASICS are custom hardware circuits. They provide the precise function needed for a specific task. Combining the flexibility of general-purpose processors and the high performance of ASICS would lead to the desired goal. Consequently, this led to the introduction of reconfigurable computing (RC). The MorphoSys is one example of an RC system, which combines a reconfigurable array of processor cells with a RISC processor core and a high bandwidth memory interface unit. This paper introduces two new coding algorithms using reconfigurable computing (RC) and specifically chooses one of the prototypes in this field, MorphoSys (M1) [Bagherzadeh, 1998]. A performance analysis study of the M1 RC is also presented to evaluate the execution efficiency of the suggested algorithms on the M1 system. The mapped algorithms deal namely with checksum coding, and linear sequential coding. Examples (64-input bytes vector on the 8x8 RC array M1) were run, to validate our results, using the MorphoSys mULATE program, which simulates MorphoSys operations.

Keywords: *Digital Coding, Checksum, Linear Sequential Circuits, Reconfigurable Computers, MorphoSys, Reconfigurable Cells, Reconfigurable Array.*

الملخص

[illegible] (ASICs) [illegible] (Reconfigurable) [illegible] (M1) [illegible] .(Reconfigurable) [illegible] (Checksum) [illegible] .(Linear Sequential Circuits) [illegible] .(mULATE)