ARCHITECTURAL MODIFICATIONS FOR OPTIMIZING MAPPINGS ON MORPHOSYS RC-SYSTEM

Issam Damaj, and Hassan Diab
id01@aub.edu.lb; diab@aub.edu.lb
American University of Beirut
Department of Electrical and Computer Engineering
Faculty of Engineering and Architecture
Beirut, Lebanon
P.O. BOX 1102

Abstract

This paper presents architectural modifications to the reconfigurable part of MorphoSys, a reconfigurable computing (RC) system [2], which improves system performance [1-6]. RC is introduced, followed by the MorphoSys (M1) RC system. Moreover, two algorithms are mapped to the system based on the enhanced interconnection scheme and ALU complexity. The algorithms include a computer graphics acceleration algorithm to which ALU enhancement to M1 was considered, and an FIR filter algorithm to which interconnection enhancement to M1 was applied. The results presented indicate an improved performance. A spreadsheet model is used to present the modification and the performance improvement. The speedup achieved is explained as well as the advantages in the mapping of the application.

Keywords Reconfigurable Computing, Parallel Algorithms, Graphics Acceleration, MorphoSys