RECONFIGURABLE HARDWARE SYNTHESIS FOR PARALLEL CYCLIC CODING ALGORITHMS

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ABSTRACT

This paper introduces the application of a rapid development model with cyclic redundancy checkers for digital coding algorithms on a reconfigurable hardware platform. The addressed model adopts the transformational programming approach for deriving massively parallel algorithms from functional specifications. The functional notation is used for specifying algorithms and for the reasoning about them. The systematic method for massive parallelisation of the algorithm works by carefully composing "off the shelf" massively parallel implementation of each of the building blocks involved in the algorithm. To describe parallelism we use Hoare's CSP. The reconfigurable hardware realization step is done using Handel-C an automated compilation development model. The targeted hardware is the RC-1000 FPGA from Celoxica. Several numerical examples were run and the performance analysis is done with comparisons among different general and reconfigurable processing systems.